introduces significant latency, frequency limitations and power requirements. To mitigate these problems, the present invention effects signalling capacitively. Preferably, pairs of half-capacitor plates, one half located on each chip, module or substrate are used to capacitively couple signals from one chip, module or substrate to another. The use of plates relaxes the area needed to effect signalling, and reduces or eliminates the requirements for exotic metallurgy.

Applicants' use of capacitive coupling to communicate signals between chip, module or substrate is distinguished in the specification from power supply connections. For example, in Fig. 1, the capacitive signal path is provided by half-capacitors 14 and 15 while the power supply is represented by contact 16. See page 25, line 16 to page 26, line 2 of applicants' specification. Likewise, in Fig. 4 signal paths are provided by half-capacitors 14 and 15 and 64 and 65, while power is supplied through contacts 52. See page 34, line 21 to page 35, line 17.

In contrast, Moresco describes the use of a bypass capacitor to reduce noise in the power supplied to an integrated circuit chip. Col. 1, lines 11-13. Moresco's by-pass capacitor shorts to AC noise to ground. As he states, "Again, one of these plates [of the bypass capacitor] must be electrically connected to ground while the other is connected to the power supply line." Col. 6, lines 26-28. In specifying these connections, it is clear that Moresco does not disclose or suggest the use of a capacitor to provide signalling between the chip and the substrate. Indeed, Moresco carefully distinguishes between signal line connections and power connections. He states:

> Various methods are available for connecting IC chips to other devices. Connections are required not only for power supply, but also for signal lines between chips, other device components and various input/output ("I/O") devices.

Col. 1, lines 45-49.

As applicants acknowledged in their response of September 9, 1996, capacitors are used extensively to reduce voltage fluctuations on power and ground planes. Applicants do not

claim that this is their invention. Rather, applicants have discovered that capacitively coupling a signal between different chips, modules, or substrates that are distinct and separate from one another obviates the need for physical connectors.

Independent claims 1, 28 and 102 all provide some recitation of this feature of applicants' invention. Claim 1 recites "means for capacitively signalling". Claim 28 recites a second half-capacitor "capacitively coupling a signal"; and claim 102 recites half-capacitors that provide "a capacitive signal path".

To further emphasize the difference between applicants' invention and Moresco et al., each of independent claims 1, 28 and 102 has been amended to add the recitation of signal leads connected to the capacitive signalling means. Support for this limitation is found, for example, in transmission lines 32, 33, 34 and 37 of Fig. 2 which are discussed at page 32, line 28 to page 33, line 12 of the specification and in the circuitry of Figs. 30, 31A, 31B and 32 discussed at page 81, line 5 to page 83, line 7.

Applicants respectfully traverse the rejection of the claims as anticipated by Moresco. In distinguishing between power connections and signal connections and in requiring that one plate of his by-pass capacitor be connected to ground while the other is connected to the power supply line, Moresco indicates that his capacitor is not being used for capacitively coupling signals.

Nor is there any suggestion in Moresco that a capacitor be used to couple signals between an integrated circuit and a substrate. Filtering to eliminate noise is not the equivalent of signalling and does not indicate that what might work for filtering purposes would work for the transmission of signals.

Since each of claims 1, 28 and 102 recites some feature of capacitive coupling of signals, each of these claims and the claims dependent thereon is believed patentable over Moresco.

For the foregoing reasons, it is submitted that the claims are patentable over the Moresco reference.

Applicants also wish to traverse the Examiner's comment that Moresco claims the applicants' invention. Since Moresco claims a specific structure in means plus function language, his claim is limited to what he discloses in his specification and equivalents thereof. This structure is essentially a dielectric film between two solder bumps. This is not applicants' invention.

For the foregoing reasons, the present application is believed to be in condition for allowance. Such action is respectfully requested.

Respectfully submitted,

Date February 25, 1998

Francis E. Morris 24,615
Francis E. Morris (Reg. No.)

PENNIE & EDMONDS LLP
1155 Avenue of the Americas
New York, New York 10036-2711
(212) 790-9090

Enclosure